VERIFICATION OF TRANSLATION

I, Woo-Hyun WHANG, of Suite 1810, Hwanghwa Bldg., 832-7, Yeoksam-dong, Gangnam-gu, Seoul, Republic of Korea hereby declare that I am knowledgeable in the English and Koean languages, and that to the best of my knowledge the attached document is a true and complete English translation of Korean Patent Application No. 10-2003-0049075.

Dated August 4, 2006

Woo-Hyun Hwang

Signature

Translation of Priority Document

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[Abstract of the Disclosure]

[Abstract]

A high-speed flat panel display having a long lifespan is provided. In the high-speed flat panel display, a thin film transistor of a pixel part in which pixels are arranged has a different resistance from a thin film transistor of a driving circuit part for driving the pixels of the pixel part.

The flat panel display includes a pixel part in which a plurality of pixels are arranged; and a driving circuit part for driving the pixels of the pixel part, wherein thin film transistors constituting the pixel part and the driving circuit part have different resistances in a gate or drain region.

At least one of the thin film transistors constituting the pixel part and the driving circuit part has an offset region in a gate region, and the offset region is a high resistance region that is entirely or partially doped with an impurity with the same conductivity type as source and drain regions at a relatively lower concentration than the source and drain regions or not doped with any impurity.

[Typical Figure]

FIG. 3B

[Specification]

[Title of the Invention]

FLAT PANEL DISPLAY

[Brief Description of the Drawings]

FIG. 1 illustrates the structure of a conventional organic light emitting display;

FIG. 2 is a plan view illustrating a thin film transistor of a driving circuit part in an organic light emitting display according to an exemplary embodiment of the invention;

FIGS. 3A and 3B are plan and cross-sectional views illustrating a thin film transistor of a pixel part in an organic light emitting display according to a first exemplary embodiment of the invention;

FIGS. 4A and 4B are plan and cross-sectional views illustrating a thin film transistor of a pixel region in an organic light emitting display according to a second exemplary embodiment of the invention; and

FIG. 5 is a plan view illustrating a thin film transistor of a pixel part in an organic light emitting display according to a third exemplary embodiment of the invention; and

FIG. 6 is a plan view illustrating a thin film transistor of a pixel part in an organic light emitting display according to a fourth exemplary embodiment of the invention.

* Explanation of the signs that are the main part of the drawings

220, 320, 420, 520, 620: semiconductor layer

240, 340, 440, 540, 640: gate

221, 321, 421, 521, 621: source region

225, 325, 425, 525, 625: drain region

251, 255, 351, 355, 451, 455, 551, 555, 651,656: contact

261, 361, 461, 561, 661: source electrode

265, 365, 465, 565, 665: drain electrode

224, 323, 327, 423, 427, 530, 650: channel region

[Detailed Description of the Invention]

[Object of the Invention]

[Field of the Invention and Prior Art related to the Invention]

The present invention relates to a full-color flat panel display, and more particularly, to a high-speed flat panel display with a long lifespan in which a thin film transistor of a pixel part has a different resistance from a thin film transistor of a driving circuit part.

In general, an organic light emitting display, a flat panel display, includes a pixel part 110 in which a plurality of pixels are arranged in a matrix form on an insulating substrate 100, and a driving circuit part for driving the pixel part 110 as shown in FIG. 1. The pixel part 100 is not shown in the figure but has multiple gate lines, multiple data lines, and multiple common power lines, and the plurality of pixels connected to these lines are arranged in a matrix form. Each pixel includes an

electroluminescent (EL) device, a driving transistor for supplying driving current in response to a data signal from the data line to the EL device, a switching transistor for transmitting a data signal to the driving transistor in response to a scan signal supplied to the gate line, and a capacitor for storing the data signals.

The driving circuit part for driving the pixels in the pixel part 110 includes a gate driving circuit part 130 for providing a scan signal enabling the gate line of the pixel part 110 to be driven, and a data driving circuit part 120 for providing a data signal to the data line of the pixel part 110.

In a conventional active matrix organic light emitting display (AMOLED), all thin film transistors which are disposed in the pixel part (100) and the driving circuit parts 120 and 130 are formed of polysilicon. In an AMOLED having a high resolution of 180 ppi or more, when the thin film transistors in the pixel and driving circuit parts are formed of polysilicon, a high-speed operation characteristic could be obtained from the driving circuit part due to high mobility of the thin film transistors. However, because of a high on-current, the amount of current flowing through the EL device of the pixel part became more than a threshold value, and thus luminance per unit area increased and the lifespan of the EL device was shortened.

Meanwhile, when the pixel part and the driving circuit part were composed of thin film transistors having low mobility in order to

maintain the on-current characteristic as necessary, on-current became relatively lower and appropriate luminance was obtained. This solved the problem of shortening of the lifespan of the EL device, but precluded attainment of the high-speed operation characteristic of the driving circuit part.

[Technical Object of the Invention]

Therefore, it is an object of the invention to provide a flat panel display having a long lifespan.

It is another object of the invention to provide a flat panel display in which pixel and driving circuit parts are composed of thin film transistors with different resistances enabling attainment of a high-speed operation characteristic and a long lifespan.

It is still another object of the invention to provide a flat panel display enabling attainment of a high-speed operation characteristic and a long lifespan by changing doping concentration of gate and drain regions of thin film transistors of pixel and driving circuit parts.

[Construction of the Invention]

One aspect of the invention provides a flat panel display including a pixel part in which a plurality of pixels are arranged, and a driving circuit part for driving the pixels of the pixel part. Thin film transistors constituting the pixel and driving circuit parts have different resistances.

At least one of the thin film transistors of the pixel part has a

larger resistance than the thin film transistors of the driving circuit part.

Another aspect of the invention provides a flat panel display including: a pixel part in which a plurality of pixels are arranged; and a driving circuit part for driving the pixels of the pixel part. Thin film transistors constituting the pixel and driving circuit parts have different resistances in a gate region.

One of the thin film transistors constituting the pixel and driving circuit parts may have an offset region in a gate region. The offset region may be a high resistance region which is entirely or partially doped with an impurity having the same conductivity type as the source and drain regions at a relatively lower concentration than the source and drain regions, or not doped with any impurity.

Still another aspect of the invention provides a flat panel display including: a pixel part in which a plurality of pixels are arranged; and a driving circuit part for driving the pixels of the pixel part. Thin film transistors constituting the pixel and driving circuit parts have different resistances at least in a drain region.

At least one of the thin film transistors constituting the pixel and driving circuit parts may include an offset region in a drain region. The offset region may be a high resistance region which is entirely or partially doped with an impurity having the same conductivity type as the drain region at a relatively lower concentration than the drain region, or not doped with any impurity.

Yet another aspect of the invention provides a flat panel display including: a pixel part in which a plurality of pixels are arranged; and gate and data driving circuit parts for driving the pixels of the pixel part. Thin film transistors of the pixel part have a different resistance from at least one of thin film transistors constituting the gate and data driving circuit parts.

The thin film transistor of the pixel part may include an offset region in a gate or drain region. The offset region may be a low resistance region which is entirely or partially doped with an impurity having the same conductivity type as the drain region at a relatively lower concentration than the drain region, or not doped with any impurity.

The present invention will now be described more fully hereinafter with reference to the attached drawings, wherein the same numerals denote the same components.

FIG. 2 is a plan view illustrating a thin film transistor of a driving circuit part in an organic light emitting display of the invention.

Referring to FIG. 2, the thin film transistor constituting the pixel part includes a semiconductor layer 220 formed of polysilicon, a gate electrode 240, and source and drain electrodes 261 and 265. The semiconductor layer 220 includes a channel region 224 corresponding to the gate electrode 240, and source and drain regions 221 and 225 formed at both sides of the channel region 224. The source and drain

electrodes 261 and 265 are electrically connected to the source and drain regions 221 and 225 through contacts 251 and 255.

FIGS. 3A and 3B illustrate a first example of a thin film transistor constituting a gate or data driving circuit part in an organic light emitting display according to an exemplary embodiment of the invention. FIG. 3A is a plan view of a thin film transistor, and FIG. 3B is a cross-sectional view of a thin film transistor taken along line 3B-B' of FIG. 3A.

Referring to FIGS. 3A and 3B, the thin film transistor of the driving circuit part includes a semiconductor layer 320, a gate electrode 340, and source and drain electrodes 361 and 365. The gate electrode 340 includes multiple gates 341 and 345 corresponding to the semiconductor layer 320.

The semiconductor layer 320 has a "ㄷ"-shaped structure which includes multiple channel regions 323 and 327 respectively corresponding to the multiple gates 341 and 345 of the gate electrode 340, and high-concentration source and drain regions 321 and 325 formed at one side of each of the channel regions 323 and 327, respectively. Also, the semiconductor layer 320 further includes an offset region 330 interposed between the multiple channel regions 323 and 327, i.e., between the multiple gates 341 and 345. The source and drain electrodes 361 and 365 are electrically connected to the high-concentration source and drain regions 321 and 325 formed in the

semiconductor layer 320 through contacts 351 and 355, respectively.

The offset region 330 is a high resistance region, which comprises a low-concentration impurity region doped with an impurity with the same conductivity type as the high-concentration source and drain regions 321 and 325 at a lower concentration than the source and drain regions 321 and 325, or an intrinsic region which is not doped with any impurity.

FIGS. 4A and 4B illustrate a second example of a thin film transistor of a pixel region in an organic light emitting display according to an exemplary embodiment of the invention. FIG. 4A is a plan view of a thin film transistor, and FIG 4B is a cross-sectional view of a thin film transistor taken along line 4B-4B' of FIG. 4A.

The resistance of the thin film transistor illustrated in FIGS. 4A and 4B is changed by altering a doping state of an offset region between multiple gates like in the first example of FIGS. 3A and 3B.

That is, the thin film transistor of the pixel part includes a "ㄷ"-shaped semiconductor layer 420, a gate electrode 440, and source and drain electrodes 461 and 465. The gate electrode 440 includes multiple gates 441 and 445 corresponding to the semiconductor layer 420. The source and drain electrodes 461 and 465 are electrically connected to high-concentration source and drain regions 421 and 425 of the semiconductor layer 420 through contacts 451 and 455, respectively.

The semiconductor layer 420 includes multiple channel regions 423 and 427 respectively corresponding to the multiple gates 441 and 445 of the gate electrode 440, and the high-concentration source and drain regions 421 and 425 formed at one side of each of the multiple channel regions 423 and 427, respectively. Also, the semiconductor layer 420 includes an offset region 430 interposed between the multiple gates 441 and 445, i.e., the multiple channel regions 423 and 427.

The offset region 430 is a high resistance offset region which comprises a part 435 doped with a low concentration impurity having the same conductivity type as the high-concentration source and drain regions 421 and 425, and an undoped part 431 between the doped parts.

According to the first and second examples, the thin film transistor of the pixel part has the high resistance offset region 430 entirely or partially doped with a low concentration impurity between multiple gates, or not doped with any impurity, and thus its resistance increases. Therefore, when the driving circuit part is composed of the thin film transistor illustrated in FIG. 2, and the pixel part is composed of the thin film transistor with a high resistance offset region interposed between the multiple gates illustrated in FIGS. 3A, 3B, 4A and 4B, the driving circuit part maintains a high-speed operation characteristic like a conventional organic light emitting display and the pixel part reduces current flowing through the EL device due to an increase in the

resistance of the thin film transistor. Accordingly, the lifespan of the device may be extended.

That is, when the gate regions in the thin film transistor of the pixel part in the first and second examples are set to be a multi-channel region under the multi gates and an offset region between the multi gates, and the gate region in the thin film transistor of the driving circuit part illustrated in FIG. 2 is set to be a channel region under the gates, the gate region in the thin film transistor of the driving circuit part may maintain the high-speed operation characteristic because of the small resistance as in the conventional thin film transistor. Meanwhile, the gate region in the thin film transistor of the pixel part has a large resistance as the shape of the offset region is altered, and thus the current flowing through the EL device may be controlled and appropriate luminance may be generated, thereby extending the device's lifespan.

FIG. 5 is a plan view illustrating a third example of a thin film transistor of a pixel part in an organic light emitting display according to an exemplary embodiment of the invention.

Referring to FIG. 5, the thin film transistor constituting the pixel part includes a semiconductor layer 520 formed of polysilicon, a gate electrode 540, and source and drain electrodes 561 and 565. The semiconductor layer 520 includes a channel region 524 corresponding to the gate electrode 540, and source and drain regions 521 and 525

formed at both sides of the channel region 524. The source and drain electrodes 561 and 565 are electrically connected to the source and drain regions 521 and 525 through contacts 551 and 555, respectively.

The semiconductor layer 520 further includes offset regions 523 and 527 between the channel region 524 and the source and drain regions 521 and 525. The offset regions 523 and 527 are high resistance regions comprising an intrinsic region not doped with any impurity.

In the thin film transistor of the pixel part according to the third example, the source and drain regions 521 and 525 include the offset regions 523 and 527, respectively. However, only the drain region 525 may have an offset region.

FIG. 6 illustrates a fourth example of a thin film transistor of a pixel part of an organic light emitting display according to an exemplary embodiment of the invention.

Referring to FIG. 6, the thin film transistor constituting the pixel part includes a semiconductor layer 620 formed of polysilicon, a gate electrode 640, and source and drain electrodes 661 and 665. The semiconductor layer 620 includes a channel region 624 corresponding to the gate electrode 640, and source and drain regions 621 and 625 formed at both sides of the channel region 624. The source and drain electrodes 661 and 665 are electrically connected to the source and drain regions 621 and 625 through contacts 651 and 655.

The semiconductor layer 620 further includes offset regions 623 and 627 between the channel region 623 and the source and drain regions 621 and 625. The offset regions 623 and 627 are high resistance regions entirely or partially doped with an impurity with the same conductivity type as the high-concentration source and drain regions 621 and 625 at a lower concentration than the high-concentration source and drain regions 621 and 625.

In the thin film transistor of the pixel part according to the fourth example, the source and drain regions 621 and 625 include the offset regions 623 and 627, respectively. However, only the drain region 625 may have an offset region.

According to the third and fourth examples, the thin film transistor of the pixel part has an offset region 627 at least in a drain region, and thus its resistance increases. Therefore, when the driving circuit part is composed of the thin film transistor as illustrated in FIG. 2, and the pixel part is composed of the thin film transistor including the drain offset region as illustrate in FIGS. 5 and 6, the driving circuit part maintains a high-speed operation characteristic like a conventional organic light emitting display and the pixel part reduces current flowing through the EL device due to an increase in the resistance of the thin film transistor, and thereby extending the device's lifespan.

That is, the resistance of the drain region of the thin film transistor of the pixel part according to the third and fourth examples is

changed depending on a doping state of the drain offset region so that the drain region of the thin film transistor of the driving circuit part has a small resistance like the conventional thin film transistor, thereby maintaining a high-speed operation characteristic. And, the drain region of the thin film transistor of the pixel part has a large resistance, thereby controlling the current flowing through the EL device and generating appropriate luminance, and thus the device's lifespan may be extended.

In the exemplary embodiments of the invention, while a thin film transistor of a pixel part has a high resistance offset region between multiple gates or in a drain region, so as to change the resistance of the thin film transistor in the pixel part depending on a doping state of the offset region and control current flowing through the EL device, the offset region may be formed in all thin film transistors constituting a pixel region or only in a corresponding thin film transistor.

A high resistance offset region according to the exemplary embodiments of the invention may be applied in all thin film transistors constituting a pixel part, or in at least one thin film transistor, for example, a thin film transistor for driving the EL device.

Though in the exemplary embodiments of the invention illustrated herein, the semiconductor layer has a "⊏"-shaped structure and the gate electrode has a dual gate, the semiconductor layer and gate can have any structure that allows the resistance of the thin film

transistor in the pixel part to be changed.

[Effects of the Invention]

According to the exemplary embodiment of the invention, a doping state of a gate or drain offset region of a thin film transistor of a pixel part is altered to change resistance, thus a high-speed operation characteristic may be obtained and a device's lifespan may be extended.

Although the invention has been described with reference to certain exemplary embodiments thereof, it will be understood by those skilled in the art that a variety of modifications and variations may be made to the invention without departing from the spirit or scope of the invention.

[Claims]

[Claim 1]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

a driving circuit part driving the pixels of the pixel part,

wherein thin film transistors constituting the pixel part and the driving circuit part have different resistances.

[Claim 2]

The flat panel display according to claim 1, wherein at least one of the thin film transistors constituting the pixel part has a larger resistance than that of the driving circuit part.

[Claim 3]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

a driving circuit part for driving the pixels of the pixel part,

wherein thin film transistors constituting the pixel part and the driving circuit part have different resistances in a gate region.

[Claim 4]

The flat panel display according to claim 3, wherein one of the thin film transistors constituting the pixel and driving circuit parts comprises an offset region in the gate region.

[Claim 5]

The flat panel display according to claim 4, wherein the one of the thin film transistors constituting the pixel and driving circuit parts comprises source and drain regions, and the offset region is a high resistance region entirely or partially doped with an impurity having the same conductivity type as the source and drain regions at a relatively lower concentration than the source and drain regions, or not doped with any impurity.

[Claim 6]

The flat panel display according to claim 3, wherein the thin film transistor having the gate offset region is at least one of the thin film transistors constituting the pixel part.

[Claim 7]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

a driving circuit part for driving the pixels of the pixel part,

wherein thin film transistors constituting the pixel part and the driving circuit part have different resistances at least in a drain region.

[Claim 8]

The flat panel display according to claim 7, wherein one of the thin film transistors constituting the pixel and driving circuit parts comprises an offset region at least in a drain region.

[Claim 9]

The flat panel display according to claim 8, wherein the offset

region in the one of the thin film transistors constituting the pixel and driving circuit parts is a high resistance region entirely or partially doped with an impurity having the same conductivity type as the drain region at a relatively lower concentration than the drain region, or not doped with any impurity.

[Claim 10]

The flat panel display according to claim 7, wherein the thin film transistor including the drain offset region is at least one of the thin film transistors constituting the pixel part.

[Claim 11]

A flat panel display, comprising:

a pixel part in which a plurality of pixels are arranged; and

gate and data driving circuit parts for driving the pixels of the pixel part,

wherein at least one of thin film transistors constituting the pixel part has a different resistance from at least one of thin film transistors constituting the gate and data driving circuit parts.

[Claim 12]

The flat panel display according to claim 11, wherein the at least one of the thin film transistors of the pixel part comprises an offset region in a gate region.

[Claim 13]

The flat panel display according to claim 12, wherein the at

least one of the thin film transistors of the pixel part comprises source and drain regions, and the offset region is a high resistance region entirely or partially doped with an impurity having the same conductivity type as the source and drain regions at a relatively lower concentration than the source and drain regions, or not doped with any impurity.

[Claim 14]

The flat panel display according to claim 11, wherein the at least one of the thin film transistors of the pixel part comprises an offset region at least in a drain region.

[Claim 15]

The flat panel display according to claim 14, wherein the offset region in the at least one of the thin film transistors of the pixel part is a high resistance region entirely or partially doped with an impurity having the same conductivity type as the drain region at a relatively lower concentration than the drain region, or not doped with any impurity.

FIG. 1

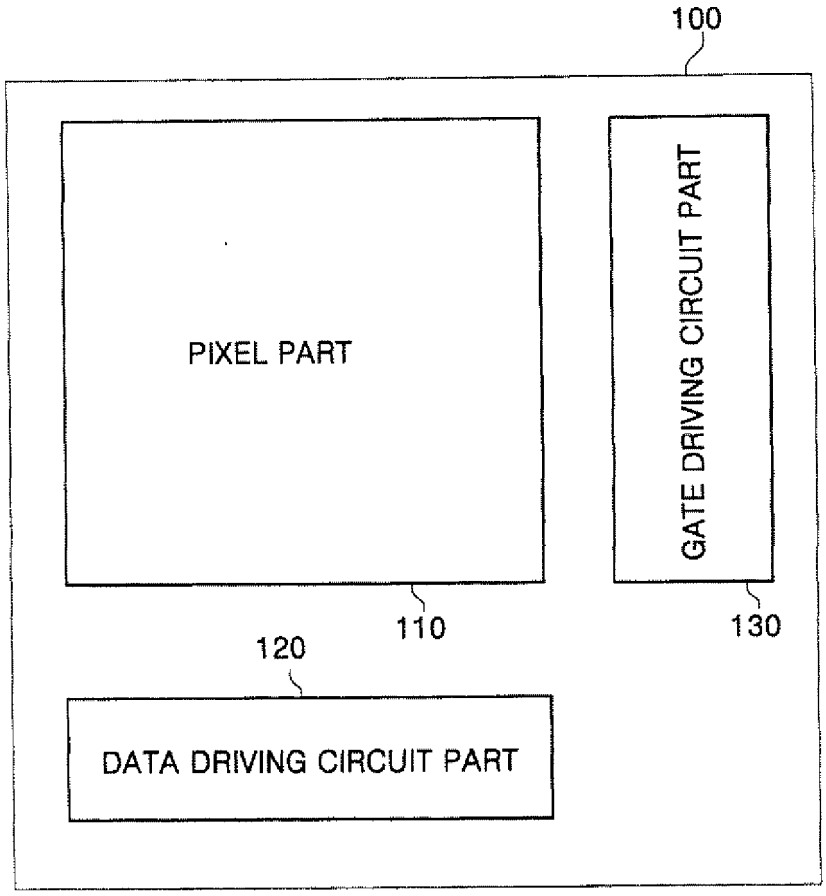

100
PIXEL PART
GATE DRIVING CIRCUIT PART
110
130
120
DATA DRIVING CIRCUIT PART

FIG. 2

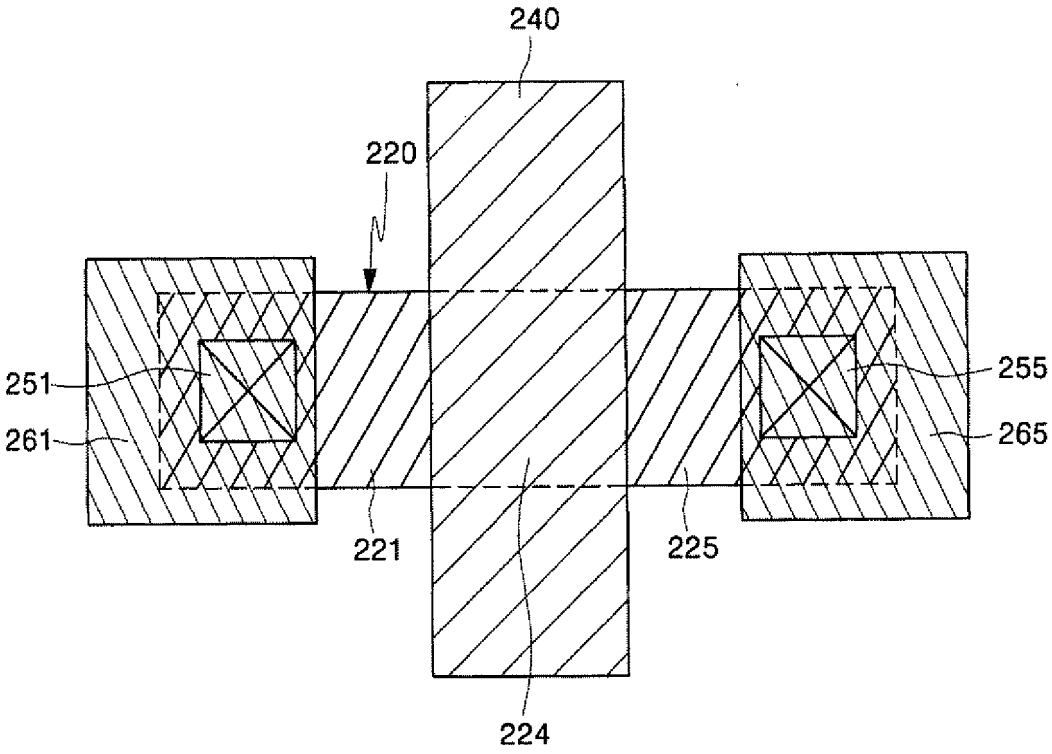
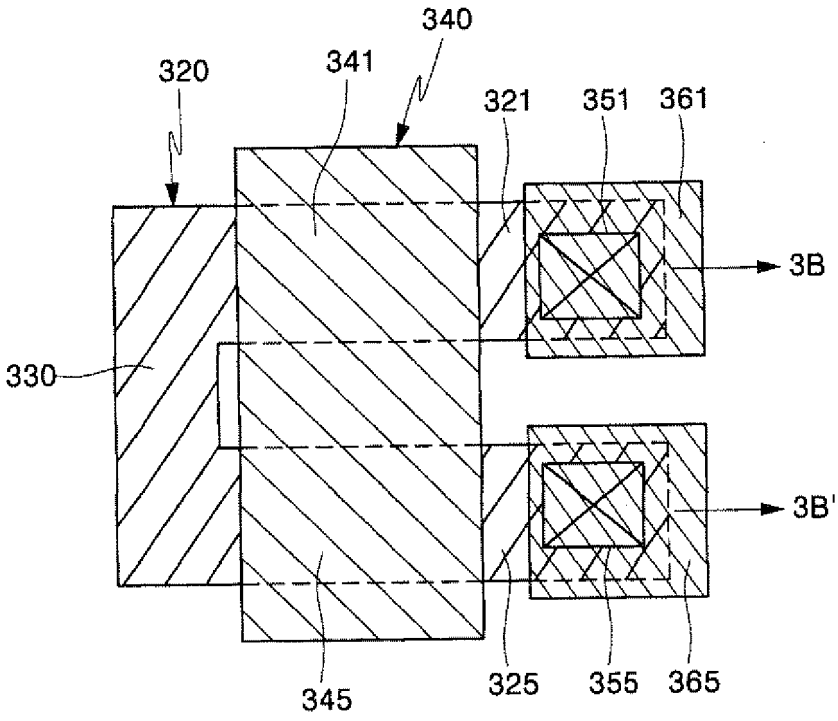


FIG. 3A


340
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341
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3B
330
3B'
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355
365

FIG. 3B

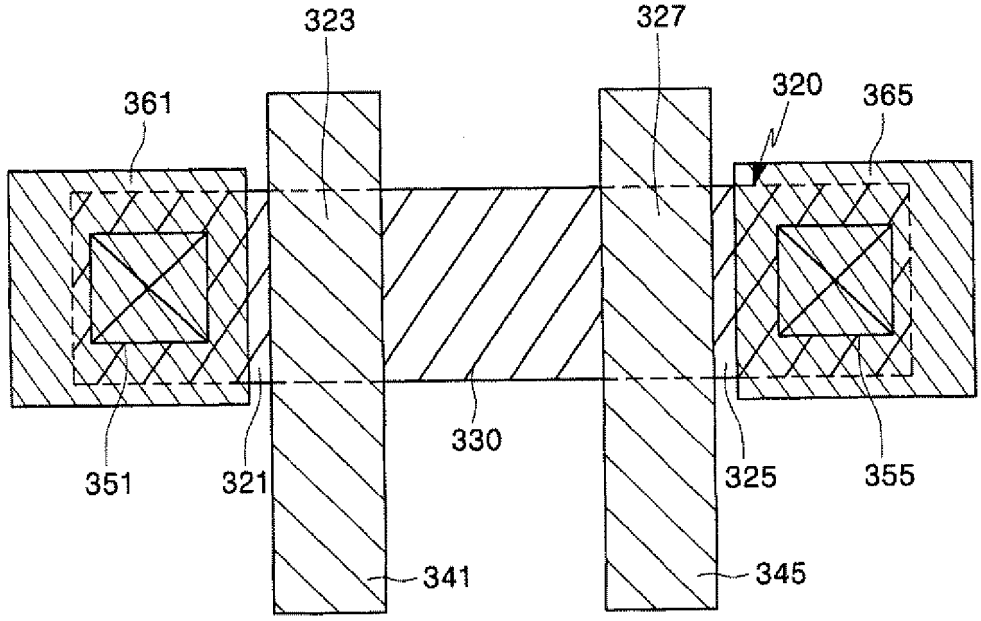
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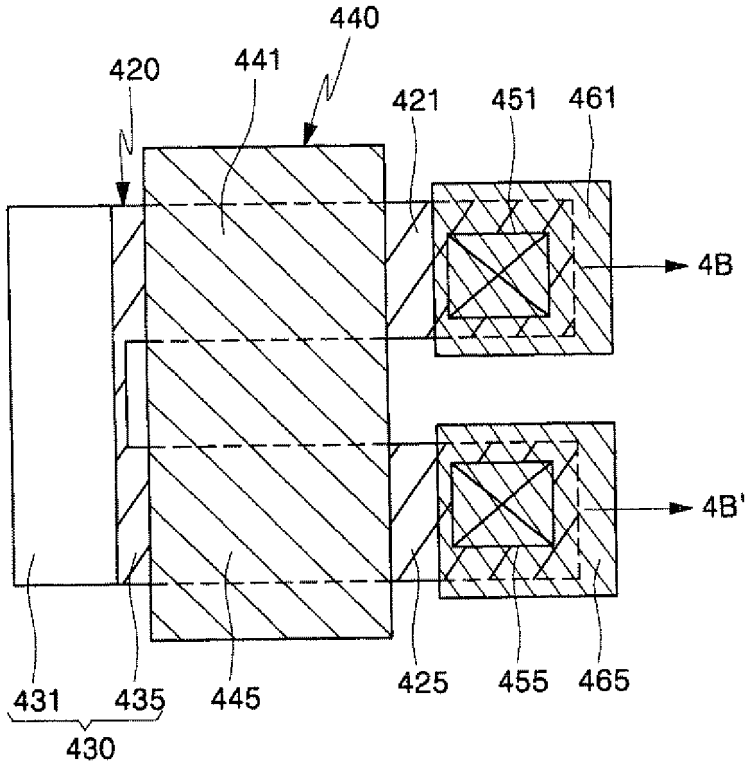
FIG. 4A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4B
4B'
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FIG. 4B

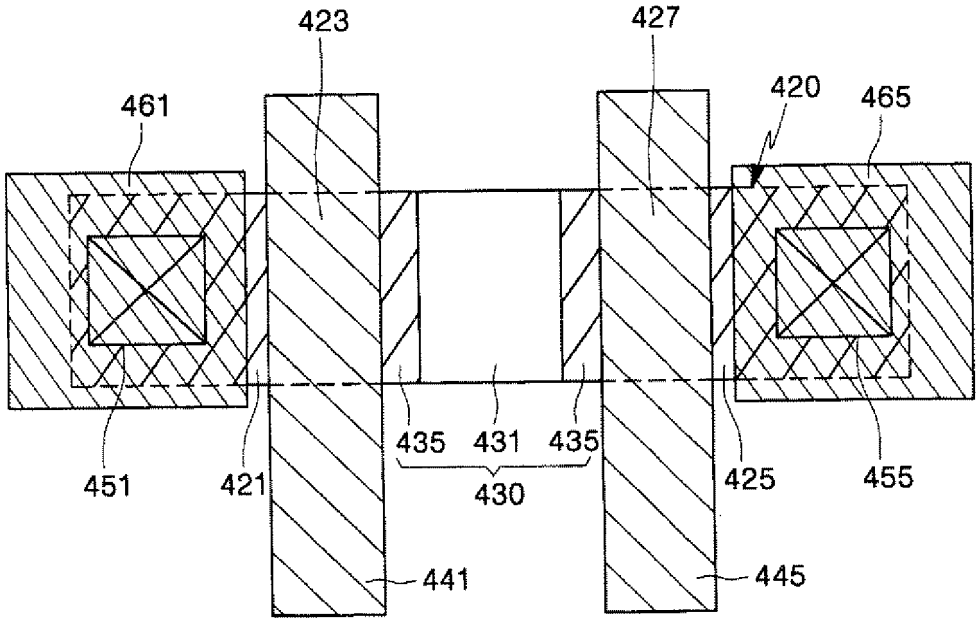
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FIG. 5

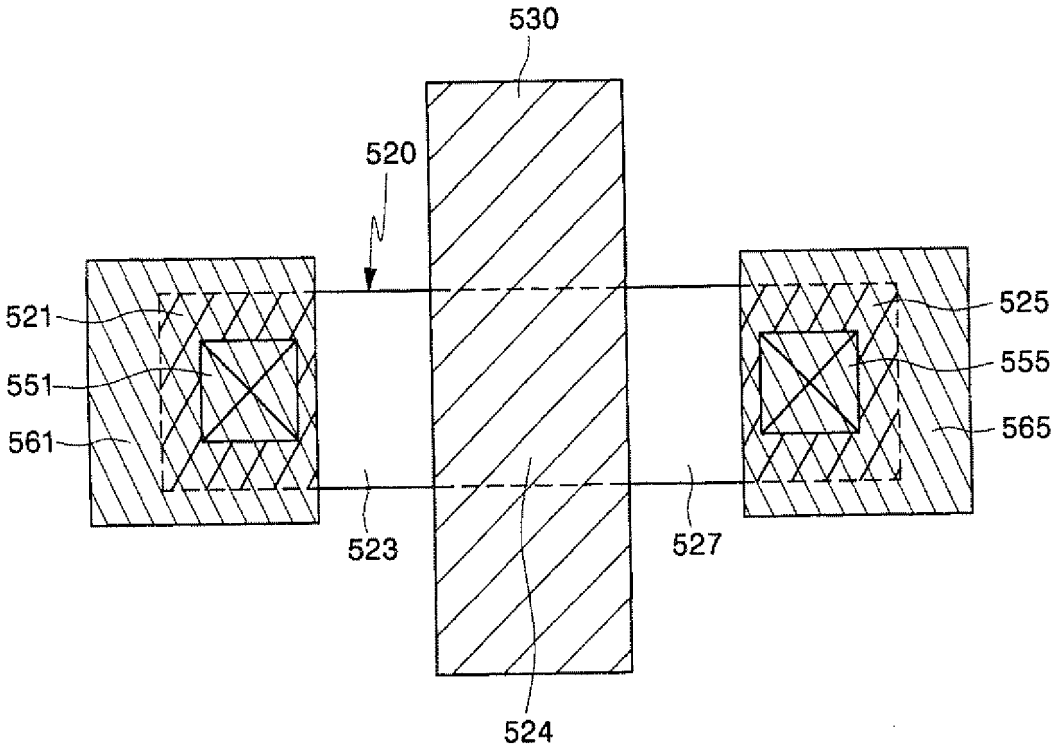
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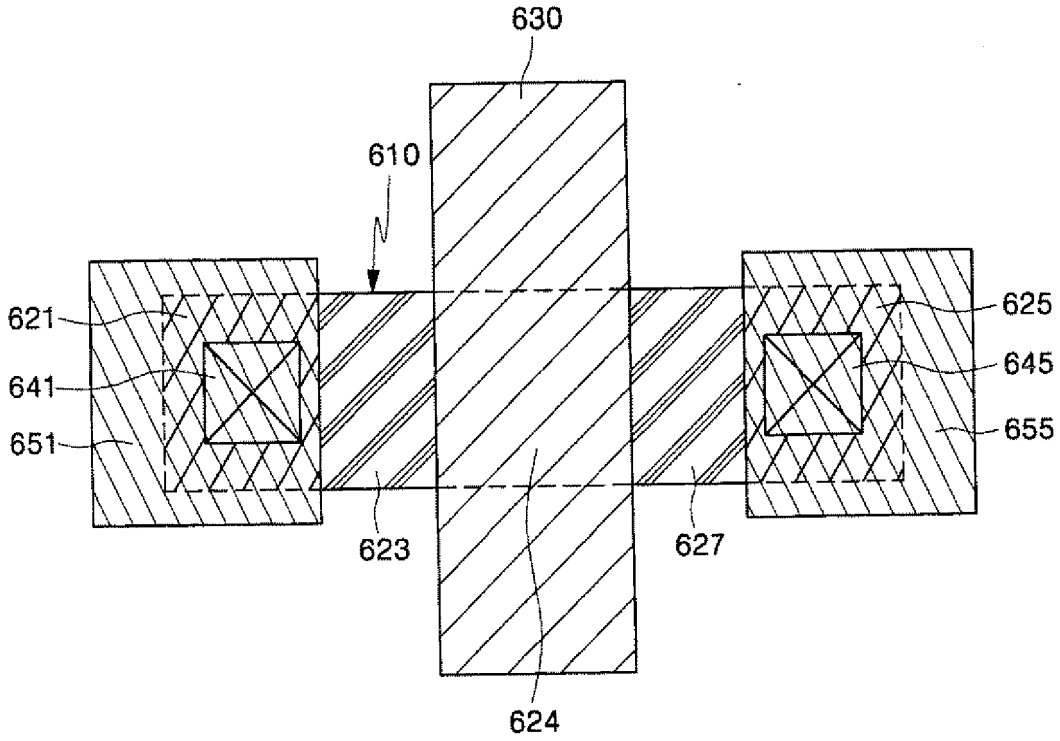
FIG. 6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